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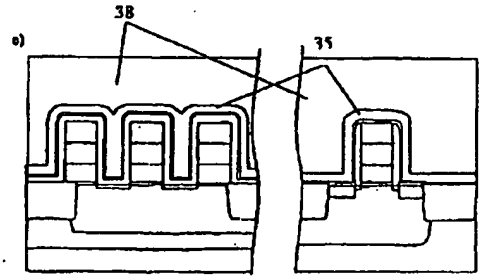
(54) MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE

(57) Abstract:

PROBLEM TO BE SOLVED: To perform nice embedding of low temperature and minute clearance of a coating process and coating separation prevention in a posterior process, for instance, in a logic memory mixed loading device or the like.

SOLUTION: The manufacturing method of a semiconductor device performs a first process for forming an insulation film by thermal CVD (chemical gas growth) on a board having on a surface a recess part made by patterning when, for instance, a BPSG film is coated and a second process forming the insulation film by thermal CVD (chemical gas growth) under pressure lower than the first process in order without continuously breaking vacuum and without interrupting the supply of a raw gas in a process from the first process to the second process.



38:BPSG膜

Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the manufacturing technology of a semiconductor device. Especially, patterning is carried out and it is related with the manufacturing technology of the semiconductor device which comes to contain the process which carries out covering formation of the insulator layer all over including the made concavo-convex field.
[0002]
[Description of the Prior Art] Quoting drawing 1 - drawing 8 , the conventional DRAM / logic mixed-loading mold semiconductor device (thing of DRAM / logic mixed-loading mold semiconductor device is only called below "mixed-loading mold semiconductor device" and "DRAM& logic".) production process are explained in order, and it moves to concrete description of the above-mentioned problem.
Refer to drawing 1 (a).
[0003] Drawing 1 is a sectional view in the middle of the production process of the conventional mixed-loading mold semiconductor device (processes a and b). In the active region demarcated by the isolation insulator layer 2 of a silicon substrate 1, wells 5 and 6 are formed n molds among drawing 1 (a), and a well 7 is formed p molds into a well 5 n molds. Furthermore, into the active region 3 of the same silicon substrate 1, and 4, the gate electrodes 10, 11, 12, and 13 of an MOS transistor carry out the laminating of for example, the polish recon film, the tungsten silicide film, and the silicon nitride film one by one, and patterning formation is carried out. The same source drain fields 15 and 16 of an MOS transistor are configurations shallowly prepared in a well 7 p mold. In addition, the left of a drawing is the DRAM section across the center section currently omitted and illustrated, and the rightist inclinations of a drawing are the logic section.
Refer to drawing 1 (b).
[0004] Next, including the front face of the gate electrodes 10, 11, 12, and 13, a silicon nitride film 20 is formed, it is made to expose, without covering only the DRAM section (left of drawing) top by the resist continuously, and covering a logic section (rightist inclinations of drawing) top by the resist, etchback clearance of this silicon nitride film 20 is carried out using dry etching, and the sidewall spacer 25 is formed only in gate electrode 10 side face of the logic section with a residual silicon nitride film in this case so that the whole surface may be covered. Then, with the resist left used as the mask, the ion implantation for source drains is performed to the substrate side of the logic section, and the source drain field 26 is selectively formed only to a logic section (rightist inclinations of drawing) active region. Subsequently, it becomes the structure which it exfoliates and shows the resist used as a mask in drawing 1 (b).
Refer to drawing 2 (c).
[0005] Then, Salicide formation of the cobalt silicide (CoSi) film 30 is carried out using technique alternative on the front face of the above mentioned logic section source drain field, and well-known in self align. Then, covering formation of the silicon nitride film 33 for using as a stopper of contact aperture opening in a next process is thinly carried out all over a substrate, and it becomes the structure shown in drawing 2 (c).
Refer to drawing 2 (d).
[0006] furthermore, said silicon nitride film 33 top -- all-out -- the BPSG film 35 -- CVD (chemical vapor deposition) -- when it forms using law, since a gate electrode spacing is a slit-like narrowly, the void 34 tends to occur in the DRAM section (left of a drawing).
Refer to drawing 3 (e).
[0007] Then, a heating reflow of the BPSG film is carried out, and a void 34 is extinguished. Although it is comparatively known for low temperature as an advantageous point that a reflow can be carried out easily, as for the BPSG film, for the positive formation of void 34 dissipation, the ****** need still produces annealing 800 degrees C or more. This temperature is later described in detail as a technical-problem point.
Refer to drawing 3 (f).
[0008] Next, opening of the contact holes 36 and 37 is carried out by dry etching, and the contact

electrodes 40 and 41 which consist of a conductor are formed in these contact holes 36 and 37 so that it may arrive even at the active region of a substrate to the BPSG film.
Refer to drawing 4 (g).
[0009] Furthermore, patterning formation of the bit line 47 is carried out so that it may connect with the contact electrodes 40 and 41 electrically through opening which formed the silicon oxide film 45 in the whole surface at uniform thickness, then was prepared into this silicon oxide film 45. The bottom of a bit line 47 is covered with the film with which the laminating of titanium night RAIDO was thinly carried out to titanium one by one.
Refer to drawing 5 (h).
[0010] Furthermore, covering formation of the silicon nitride film 49 is carried out on the whole surface including said bit line 47 front face. plasma CVD (chemical vapor deposition) -- since it is exposed to the plasma which can shave a silicon nitride film 49, a tungsten expresses, and this uses in a plasma-CVD process according to a spatter operation of argon gas in case the plasma oxidation film 48 is deposited on a bit line 47 using law, a tungsten front face will oxidize, and the tungstic-acid ghost 44 will be formed so that it may be illustrated. Then, covering formation of the plasma oxidation film 48 is carried out on the whole surface.
Refer to drawing 6 (i).
[0011] Then, into the plasma oxidation film 48, opening of the deep contact aperture is carried out in dry etching, and the amorphous silicon plug 50 is formed so that the inside of this contact aperture may be filled further, so that contact electrode 41 front face which has not connected with a bit line 47 may be exposed.
Refer to drawing 7 (j).
[0012] Subsequently, a memory cell capacitor is formed so that it may connect with the above mentioned amorphous silicon plug 50. This process is that form and carry out patterning of the ingredient layer of a dielectric layer 52 all over forming the ingredient layer of the are recording electrode 51 completely, it carrying out patterning on the plasma oxidation film 48 first, and considering as the are recording electrode 51, then the are recording electrode 51 being included, and form the ingredient layer of a counterelectrode 53 completely and it carries out patterning in piles, and forms memory cell capacitor structure. Then, the plasma oxidation silicon film 58 is formed in the whole surface sufficiently thickly including memory cell capacitor structure, and the structure of drawing 7 (j) is completed.
Refer to drawing 8 (k).
[0013] Next, it shifts to the formation process of a metal multilayer-interconnection layer.
[0014] Opening of the contact aperture 60 is deeply carried out until it arrives at a logic section (rightist inclinations of drawing) active region from plasma oxidation silicon film 58 front face which carried out covering formation at the front process. The contact aperture 60 can carry out opening using the technique which is carried out to the photolithography method combining dry etching and which is used widely. What is necessary is to carry out covering formation of the barrier metal layer 61 thinly, to embed and form the electric conduction film in the whole surface further, and just to consider as a wiring layer so that it may extend on plasma oxidation silicon film 58 external front face from the inner surface of this contact aperture 60 after an opening process. The above is the outline of the conventional technique.
[0015] By the way, since some troubles are found in such a conventional technique, they are solved in order below.
[0016] First, although to make a void as small as possible from the time of membrane formation by making comparatively high the pressure in the middle of membrane formation is tried in the covering formation process of the BPSG film explained using drawing 2 (d), if a pressure is made high, it will be known that a membrane formation rate will fall in connection with it, forming the BPSG film used as a thick interlayer insulation film at such a low membrane formation rate has low productivity, and it is not applicable to a mass production process. On the other hand, if it is going to carry out mass production application and a membrane formation rate is made high from the beginning, what the void which

remained greatly tends to disappear by the addition of sufficient heating reflow process will be considered, but since the following problems are caused, it is not desirable to fully carry out a heating reflow of the BPSG film.

[0017] Although a nitride is used widely as a dirty stopper in the case of the dry etching for ****** in an after [the one] process, if the BPSG film is arranged right above [of a nitride] thru/or directly under and each touches, the stress difference of Hazama, both, will be large, stress will be stored into both film, and a crack and a bubble-like defect will occur in both film.

[0018] If direct attachment of the BPSG film and the plasma silicon nitride film is carried out, in case it will be known in the plasma silicon nitride film that a crack will arise and the laminating of the BPSG film and the plasma silicon nitride film will be carried out to order as the cure, preparing the buffer film in an interface is known. However, if the BPSG film, the buffer film, and a plasma silicon nitride film are formed in order, on the whole, comp RESSHIBU, i.e., compressive stress, will work [the film], and a center section will be distorted with convex [some]. Then, if heat is added in this layer system, on the whole, ten sill stress, i.e., a tensile stress, will commit the film, and a center section will be distorted with convex [some]. At this time, the BPSG film is softened in response to the effect of heating. Then, when a layer system is cooled again and it returns to the original temperature, at the time of a temperature fall, ten sill stress (tensile stress) arises in a plasma silicon nitride film, comp RESSHIBU stress (compressive stress) arises on the BPSG film, and an excessive stress difference arises in the BPSG film. It tends to be amplified with the buffer film, by the time it solidifies from a softening condition, a bubble will occur inside the BPSG film, and the stress involved in such the heat history has the problem that this will remain into the film at the time of cold energy.

[0019] The 2 and heating reflow of long duration also have an adverse effect called ********** from the good to an active region, a gate electrode, etc. An elevated-temperature reflow in the object for which the BPSG film will cancel a void if it becomes when an aspect ratio (pair frontage width-of-face ratio of the depth) is one or less shallow large contact aperture of a frontage is not required, but ** can also be used as an interlayer insulation film as it is, if it is general that embedding is made, it is the object of membranous eburnation and heating of about at most 700 degrees C is performed. However, since the component field itself to which a heating reflow must be further performed for a long time for the activity of a contact aperture with a frontage it is deep and narrow in which an aspect ratio exceeds 1 coming to become unescapable with detailed-izing of a device and high integration, and erasing a void, and unnecessary impurity diffusion happens simultaneously is made detailed, the adverse effect of the impurity diffusion by the heating reflow is unfathomable.

[0020] Although the above is a problem resulting from a heating reflow, in case it is going to cancel these, the time of crevice embedding completion embeds slowly by the high pressure so that a void may become small, and it forms subsequently sufficiently thickly, carrying out covering formation at a high deposition rate with a low pressure is also considered. However, in the middle of the boundary section for a part for the coat in the first high voltage process, and the coat in a next low voltage process, i.e., the BPSG film, if such technique is adopted as heat CVD formation of the insulator layer which contains a conductive impurity like the BPSG film, a clear volume phase will be made. Although opening of the contact aperture for letting wiring formed that it should connect with the active region and the electric target in the substrate below the BPSG film pass is carried out to the BPSG film used as an interlayer insulation film after such a volume phase is formed, covering formation of the wiring layer is not suddenly carried out into a contact-after opening aperture, it exposes to a drug solution that the base of an aperture should once be defecated, and wet etching is carried out lightly. The drug solution (etchant) used at this process tends to sink into the aforementioned volume phase from the side face of an aperture, and exfoliation tends to be caused later.

[0021] Incidentally, if the BPSG film is formed under a steam ambient atmosphere, it carries out a reflow also at comparatively low temperature and is desirable, but in order to prevent oxidation of the front face by the steam when using refractory metals, such as a tungsten, for a part of layer if it heats under a steam ambient atmosphere, the need of preparing the liner film which consists of a damp-proof high low voltage CVD-silicon nitride (LP-CVD SiN film) comes out. However, preparing bit line

Hazama a silicon nitride with a high dielectric constant also has the problem that the liner film which may raise bit line Hazama capacity, and may serve as fetters of high-speed-operation-izing, and consists of a silicon nitride checks opening with a beautiful thin contact aperture, and there is difficulty also in carrying out simple adoption of the process which performs the BPSG film under a steam ambient atmosphere technically. By the way, if it replaces with the BPSG film and the silicon oxide film (HDP-SiO2 film) using the high density plasma is used, membrane formation temperature can be low-temperature-ized at 500 degrees C or less. However, in the manufacture process using the growth gas of SiH4, O2, and Ar system used widely by membrane formation of HDP-SiO2 film, peeling will be produced in an interface with the metallic material in which inert gas, such as Ar used for membrane formation, carries out degasifying suddenly at a next heating process and it turns [a metallic material] a laminating up. Although there is also a method of changing thinking, raising the high impurity concentration in the film of the BPSG film, and aiming at membrane formation low temperature-ization Since the hygroscopicity of the BPSG film increases only in the part which is high high impurity concentration, it becomes easy to inhale the etchant at the time of the wet etching processing for natural oxidation film clearance etc., and this tends to generate the hydrate of the phosphorus called ****. If solution down stream processing is added and **** is not removed certainly, there is also a problem that residual **** serves as a foreign matter and may cause a poor pattern.

[0022]

[Problem(s) to be Solved by the Invention] As mentioned above, although the problem of a heating reflow is solvable if the coat of the insulator layer containing a conductive impurity is cut and divided into two processes of having changed conditions, a volume phase will be formed in the case of condition modification, and there is a problem from which this causes exfoliation after an after process. Although the problem of a volume phase will be lost since there is no need for a condition end reason if the heating reflow of long duration is performed enough, stress is stored into a part with the long heat history, and the film, unnecessary impurity diffusion is caused, or a problem arises variously.

[0023] Based on the situation which surround the above conventional techniques, even if the insulator layer containing a conductive impurity is used for the technical problem which this invention tends to solve, it is to offer the insulator layer coat technique which can embed narrow-ized spacing finely and in which mass production application is possible.

[0024]

[Means for Solving the Problem] Let the following configuration be a means as above-mentioned The means for solving a technical problem in this invention.

[0025] The first process which carries out heat CVD (chemical vapor deposition) formation of the insulator layer on the substrate which has the crevice made by carrying out patterning as the first means of this invention on a front face, After said insulator layer fills said crevice substantially through the first process, rather than it can set at said first process under a low pressure The manufacture approach of the semiconductor device performed in order, without breaking a vacuum continuously without interrupting supply of the material gas which uses the second process which carries out heat CVD (chemical vapor deposition) formation of the insulator layer in the process in which it results [from said first process] in said second process.

[0026] In addition, in the first means of the above, it is good as coming to contain B (boron) and P (Lynn) in [both] said insulator layer. Moreover, said insulator layer has [600 or more Torrs and the growth pressure in the second process] a good growth pressure in the first process also as being 600 or less Torrs and being characterized by membrane formation by the alkoxyl compound and ozone of alkoxysilane and said conductive impurity. Furthermore, it is good also as being characterized by carrying out a heating reflow of said insulator layer in a steam content ambient atmosphere 750 degrees C or less. Furthermore, in the approach of forming said insulator layer, it is good also considering the concentration of the total amount of said B (boron) and said P (Lynn) in the growth film in the first process as more than 24mol%.

[0027] So that the clearance formed by the wrap insulator layer in (1) gate electrode, a gate electrode side attachment wall, a conductive layer, and a field insulator layer may be embedded as the second

means of this invention the process which carries out covering formation of the silicon system insulator layer containing oxygen, and (2) -- with the process which forms the contact aperture for performing substrate contact into said insulator layer (3) -- the process which embeds a contact electrode in said contact aperture, and (4) -- with the process which forms the silicon system insulator layer containing nitrogen on said contact electrode (5) The manufacture approach of a semiconductor device of having in order the process which forms the electrode containing a refractory metal on said silicon system insulator layer, and the process which forms the silicon system insulator layer containing oxygen on said electrode using the high density plasma-CVD method which does not contain (6) inert gas in growth gas.

[0028] the second means of the above -- setting -- said process (4) -- setting -- stress -- two or less - 1.5x109 dyns/cm -- with a refractive indexes of 1.5 or more silicon -- it is good also as considering as the rich plasma oxidation film. Moreover, in said process (5), it is good also as performing RTA (rapid thermal annealing) processing in 800 degrees C or less and nitrogen-gas-atmosphere mind after the drug solution after etching for said electrode formation, or as etching after treatment, and rinsing processing.

[0029] It is the manufacture approach of a semiconductor device of having the process which forms the silicon system insulator layer containing oxygen by the high density plasma-CVD method all over a substrate including said capacitor structure front face so that said capacitor structure may be buried, without considering as the process which carries out patterning formation of the capacitor structure which consists of a capacitor electrode and a capacitor insulator layer as the third means of this invention, and the growth temperature of 500 degrees C or less, and including inert gas in growth gas.

[0030] Then, it explains below about an operation and principle of this invention.

[0031] In carrying out covering formation of the conductive impurity content insulator layer, and embedding a slit in law, Heat CVD (chemical vapor deposition) -- For example, the problem by which a very thin volume phase will be formed into the film when process conditions are changed in the middle of membrane formation so that a pressure may be made low after making the pressure high and embedding it until it embedded the case of the insulator layer which comes to contain a conductive impurity, for example, the BPSG film, and the BSG film -- dramatically -- remarkable -- appearing -- wet etchant -- sinking in -- it is so serious that it results even in exfoliation. The cause of the problem is considered that it will be related that the presentation ratios of residue at the time of stopping gas differ substantially the inside of the coat which passes gas, and is conjectured that the effect by the part with a complicated presentation and residual gas probably looks large in a conductive impurity content insulator layer like the BPSG film or the BSG film. Moreover, in the case of a heat CVD method, in the case of a plasma-CVD method, since membrane formation conditions will not be ready if an RF generator is shut off so that the plasma may not arise, there cannot be no formation of a volume phase in order that there may be residue of gas how, but before severing gas, it is substantially impossible to shift to the conditions of not forming membranes, in modification of other parameters, and if gas is turned off, formation of a volume phase will not be avoided. So, by this invention, formation of a volume phase is prevented by changing only a pressure for the gas used as a membrane formation raw material with a sink continuously. Since a volume phase is not made, etchant cannot sink in after ****** at an after process, therefore exfoliation is not caused.

[0032] Below, in accordance with a production process, it explains in more detail.

Refer to drawing 9 thru/or drawing 17 .

[0033] Each of drawing 9 thru/or drawing 17 is the sectional views in the middle of the production process of the mixed-loading mold semiconductor device in alignment with 1 operation gestalt of this invention, and is illustrated in accordance with a process in order. In this invention, as shown in drawing 9 thru/or drawing 17 , in case the BPSG film is formed in the clearance formed with the sidewall film on a gate electrode, and the silicon nitride film for dirty stoppers, the void made after growth in a clearance is canceled thru/or controlled by being [pressure / growth] high in TEOS/O3 ratio in the high pressure region of 600 or more Torrs, growing up only the thickness which fills and puts a clearance on the conditions that a growth rate is slow, and performing embedding at the 1st step. It is high in TEOS/O3 ratio, and by making a growth rate late, it becomes the conditions near a ********** rule and

membrane formation coverage is improved. However, in the above-mentioned conditions, since the growth rate is slow, since it is improvement in a throughput, a growth pressure is lower than the 1st step at the 2nd step, and it grows up on the conditions that a growth rate is high. Although reflow heating is performed after that, at least to a four or more-aspect clearance, an elevated temperature 750 degrees C or more is required of annealing in the inside of nitrogen and an oxygen ambient atmosphere. Then, it becomes possible by heating in the ambient atmosphere containing moisture to carry out a reflow and to embed at the temperature of 700 degrees C. When the OH radical in moisture cuts the network structure in an oxide film at low temperature more, it thinks for the BPSG film to carry out a reflow at lower temperature. Moreover, also in the case of heating [in the ambient atmosphere containing the above-mentioned moisture], when a growth pressure does not perform embedding in the high conditions that a growth rate is low, at the 1st step, the slit void formed after growth to the clearance between aspects 4 will become large, and a void will remain at a reflow 750 degrees C or less. If a void occurs, the short circuit between contact plugs with the substrate formed after that may be caused. Therefore, it is necessary to possess [as opposed to / at least / the embedding of a four or more-aspect clearance] continuous-process-izing of growth conditions, and heating of 750 degrees C or less in the ambient atmosphere containing moisture as conditions. By using the above-mentioned combination, process temperature can be reduced to 750 degrees C or less, diffusion of B (boron) to the inside of gate oxide can be controlled, and Vth (threshold) property fluctuation can be controlled.

[0034] When carrying out the laminating of the silicon nitride to the upper layer of the BPSG film for the object, such as a dirty stopper, a crack will occur in a nitride according to the film stress difference of a nitride and the BPSG film. Therefore, the buffer film is needed between the BPSG film and a nitride. If heat treatment is added where the laminating of the buffer film, the silicon nitride film, etc. is carried out on the BPSG film when the usual plasma oxidation film is used for the buffer film, a bubble-like defect will be produced on the BPSG film because the BPSG film absorbs big stress fluctuation of a silicon nitride film. on the other hand, the film stress of the buffer film -- two or less -1.5x109 dyns/cm silicon -- when it is the rich plasma oxidation film, bubble-like defective generating in the BPSG film after heat treatment and crack initiation can be controlled.

[0035] Furthermore, if this invention is applied to a mixed-loading device like DRAM& logic, the still more nearly following operations will be acquired secondarily. In fill uping a conductive ingredient with the DRAM section in a contact aperture and performing bit wiring, after preparing the contact plug which once takes electrical installation with the active region of a substrate, it is general to relay electrical installation to this contact plug through stack beer, and to consider as the electrical installation from the active region of a substrate. Therefore, the problem on which there is no need of carrying out opening of the deep contact aperture of a high aspect ratio until it arrives at the active region of a substrate at a stretch, from the first, and the DRAM section does not take a dirty stopper for the dry etching at the time of opening, but ** also increases junction leak cannot be started. However, in the DRAM& logic mixed-loading device which makes the logic section live together in a substrate, a situation is a little different. In a mixed-loading device, if silicide, such as cobalt silicide (CoSi), is used in the logic section for the reduction in resistance, after taking contact to the active region of a substrate at the time of bit line formation, in the DRAM section, the problem on which it ruins that a capacitor process takes long elevated-temperature heat treatment, and contact resistance of cobalt silicide (CoSi) and contact metal (sequential cascade screen of Ti/TiN/W) goes up will occur. If the structure which it is known that the contact to cobalt silicide (CoSi) is generally deficient in thermal stability, therefore adopts a stack capacitor is adopted at all, the structure of taking the active region of a substrate and contact soon is needed at a stretch by the deep contact aperture. In order to have to form an aspectual high contact aperture dramatically, and to prevent the junction leak buildup by the over etching in the cobalt silicide (CoSi) contact section, the silicon nitride film (SiN) of a stopper becomes indispensable. However, if a stopper is employed at all, since the laminating of the SiN film is carried out also like the DRAM section, the gap of the DRAM section becomes narrow, and embedding becomes severe. Even when embedding conditions cannot leave the elevated-temperature heat history severely like a DRAM& logic mixed-loading device according to this invention, the point that the device of a property good

[without worsening the yield] can be completed, and effectiveness are high.
[0036]
[Embodiment of the Invention] Again, it is drawing 9 thru/or referring to drawing 17 .
[0037] Hereafter, a production process is explained in order by making into an example the case where it applies with a DRAM& logic mixed-loading device, carrying out the sequential citation of drawing 9 thru/or drawing 17 .
In the drawing 9 reference process (a), it grows up in 100nm (LP-SiN) of heat silicon nitride films after 5nm growth as an initial heat oxide film (I-Ox) on a silicon substrate 1. Then, patterning is carried out using a photoresist and a heat nitride (LP-SiN) is etched by dry etching. Heat silicon nitride film in which patterning was done by Usher after resist clearance (LP-SiN) It is made a hard surface mask blank and trench etching of the silicon section is carried out. The etching depth is set to 400nm as an example. The HDP oxide film 2 is embedded after 10nm growth by the thermal oxidation film, and Si trench section is embedded for a trench side attachment wall by 700nm. The embedding conditions of the HDP oxide film 2 grow in SiH4/O2/helium=150/300/325sccm as an example. Then, using CMP (chemical machinery-polish), LP-SiN is used as a dirty stopper, and the HDP oxide film on SiN is removed, flattening is performed, and it considers as the shallow trench isolation (STI; isolation insulator layer) 2. furthermore, silicon substrate 1 front face demarcated by said isolation insulator layer 2 -- a conductive impurity -- introducing -- p mold -- a well 5 and n mold -- a well 6 and p mold -- a well 7 is fixed. According to cases, such as drawing 1 , the rightist inclinations of a drawing are the logic section, and the left of a drawing is the DRAM section. Furthermore, polish recon (Poly Si) 100nm, 100nm (WSi) of tungsten silicide layers, After carrying out the laminating of the 100nm (HTO) of the elevated-temperature thermal oxidation film all over a substrate one by one, by the dry etching which used the photoresist for the mask, patterning of these laminatings is carried out and it considers as a gate electrode. Following gate electrode patterning, for LDD formation, arsenic (As) is introduced into a mask for the logic section gate electrode 10 that an n channel transistor should be formed, and the ion implantation of the DRAM section gate electrodes 11, 12, and 13 is carried out [that a p channel transistor should be formed], respectively that boron (B) should be introduced into a mask. In this way, the source drain field 15 is formed in the logic section active region 4, and the source drain field 16 is formed in the DRAM section active region 3.
Then, refer to drawing 9 .
[0038] In a process (b), 2060nm (LP-SiN) of heat silicon nitride films is formed all over including said gate electrode surface on a gate electrode. In the DRAM section (left of a drawing), for the cure against an electric short circuit in SAC (self aryne contact) etching, it is not performing sidewall etchback but performing patterning, using a photoresist as a mask, and only the logic section performs sidewall etchback. In this way, in the DRAM section, a gate electrode is thoroughly covered with the heat silicon nitride film 20, and, on the other hand, can do structure where the sidewall spacer film 25 remains only in a gate electrode side face, in the logic section. Next, the source drain field 26 is selectively formed in the logic section by using the sidewall spacer film 25 as a mask.
Refer to drawing 10 .
[0039] In a process (c), in order to carry out SAISAIDO formation of the cobalt silicide (CoSi) selectively on the source drain field front face of the logic section which the silicon substrate surface exposed first, cobalt (Co) is used for a target, 10nm of cobalt (Co) film is formed all over a substrate in sputtering, it is made to combine with the silicon which forms a substrate by 500-degree C RTA (rapid thermal annealing) processing, and cobalt silicide (CoSi) 30 is formed. RTA (rapid thermal annealing) processing is performed between 500 degrees C and 30sec in the ambient atmosphere of for example, nitrogen (N2) 10?/min. Then, the 25nm heat silicon nitride film (LP-SiN) 33 is formed as the silicon nitride film used as the stopper film in the case of SAC etching of the DRAM section, and an etching stopper at the time of contact fenestration with cobalt silicide (CoSi). This heat silicon nitride film (LP-SiN) 33 needs reduction of a thermal budget because of reservation of the transistor characteristics of the logic section, and is formed using an end-fire array furnace by the growth temperature which is 700 degrees C, and the system of SiH4 / NH3/N2. The thickness of 25nm of the heat silicon nitride film (LP-

SiN) 33 is indispensable in order to prevent ****** by local over-etching by dispersion in an interlayer film. The gate inter-electrode minimum gap in the DRAM section which does not perform sidewall etchback with the above-mentioned heat silicon nitride film (LP-SiN) 33 is 70nm in width of face. The aspect ratio (pair width-of-window ratio of the depth of an aperture) of a gap part is set to 4.2 to height of 300nm of a gate electrode.

[0040] Next, it moves to a process (d) and 100nm of BPSG film 35 is first formed as film embedded about the above-mentioned gap. the growth conditions in this case -- for example, TEOS/TEP/TEOB=300/80/35mgm, O3-/helium=4000/6000sccm, growth pressure 600Torr, the growth temperature of 480 degrees C, boron (B), and Lynn -- concentration of (P) is performed at 5.0wt% 4.0wt (s)%, respectively. The growth rates at that time are 60 nm/min.

Refer to drawing 11 .

[0041] Then, at a process (e), conditions are changed and 900nm of BPSG film 38 is formed. growth conditions -- for example, TEOS/TEP/TEOB=600/195/47mgm, O3-/helium=4000/6000sccm, growth pressure 200Torr, the growth temperature of 480 degrees C, boron (B), and Lynn -- concentration of (P) is performed at 5.0wt% 4.0wt(s)%, respectively. The growth rates at that time are 350 nm/min. In this condition, it is in the condition that the joint which is made at the time of growth and formed from both the sides between the gates remained. Reflow heat-treatment between 20min is performed in a 700-degree C steam ambient atmosphere using a furnace after that. The conditions of reflow heating perform hydrogen (H2) 10?/min, and oxygen (O2) 5?/min on a steam (H2O) ambient atmosphere and 700-degree C conditions using a pie ROJIE nick for example, using an end-fire array diffusion furnace. A joint pastes up by said reflow heat-treatment. Moreover, since a reflow is produced in said low-temperature field, it is necessary to carry out concentration measured in the total amount of (Boron B) Lynn (P) more than 24mol%. A void cannot be lost, even if a void will become large and will follow the above-mentioned best conditions at the above mentioned process (d) of BPSG film 35 membrane formation, if coat nature is bad. Flattening is performed using a CMP (chemical machinery polish) process after that, and the structure shown in drawing 11 is done.

Refer to drawing 18 .

[0042] Drawing 18 is drawing showing the relation between the pressure under BPSG film formation by Heat CVD, and a membrane formation rate, and is a graph which takes a membrane formation rate (a part for nm/) along the pressure (Torr) under membrane formation on an axis of abscissa, and an axis of ordinate, and shows the change. A membrane formation rate is in a low inclination as high voltage conditions as highly as low voltage conditions as shown in this drawing 18 , but by 600 or more Torrs of pressures, even if it makes a pressure increase, a membrane formation rate seldom changes. In addition, since the change in a membrane formation rate and the size of the void made in a clearance are in a negative correlation, even if it transposes an axis of ordinate to the size (it is void smallness about the bottom of void size and an axis of ordinate in an axis-of-ordinate top) of a void, the same inclination as the graph of drawing 18 is accepted.

Refer to drawing 12 .

[0043] Next, it moves to a process (f) and spreading formation of the photoresist is carried out in the flat front face of the BPSG film 37. It uses as a mask, and a silicon nitride film (SiN) is used as a stopper, patterning of this photoresist is carried out using a well-known photolithography technique, and it carries out [only the DRAM section carries out dry etching of the contact apertures 36 and 37, and] opening.

[0044] At the continuing process (g), conductive polish recon (Poly-Si) is embedded in said contact aperture 36 and 37 using a CVD method, and electric contact to a substrate is performed. Conductive polish recon embeds said contact apertures 36 and 37, 1 ** forms, and after that, through a CMP (chemical machinery-polish) process, etchback of it is carried out and it is taken as the polish recon plugs 40 and 41 at more than sufficient thickness so that BPSG film 38 front face and a front face may continue.

Refer to drawing 13 .

[0045] a process (h) -- the front face of the structure of the remainder in the process of until said --

plasma CVD (chemical vapor deposition) -- the silicon oxide film 45 is completely formed using law. Film stress needs to be [two or less -1.5x109 dyns/cm and the refractive index of this film] 1.5 or more because of bubble-like defective control of the BPSG film. Growth conditions are for example, SiH4 154 cc/min, N2 3800 cc/min, N2O 3800 cc/min, 400kHz LF power 90W, 13.56MHz HF power 300W, and a growth pressure. 1.6Torr, growth temperature of 400 degrees C.

[0046] Then, the contact aperture for connecting with said polish recon plug and electric target using a resist mask is formed into the silicon oxide film 45. Then, the laminating of titanium (PVD-Ti) 20nm formed using the sputtering method, titanium tungsten (CVD-TiN) 20nm formed using a CVD method, (Tungsten W) 100nm, and the 60nm (ARC-SiON) of the silicon oxidation nitrides formed as an antireflection film is carried out one by one. Patterning of said laminating is carried out in the dry etching using a resist mask after that, and it considers as a bit line 47.

Refer to drawing 14 .

[0047] At the continuing process (i), RTA (rapid thermal annealing) processing in nitrogen-gas-atmosphere mind (5nm or 800 degrees C or less) is performed for a heat silicon nitride film (LP-SiN) 60 secs on said bit line 47, and covering formation of the silicon nitride film 49 is carried out on titanium (Ti) and a tungsten (W) front face. Then, 750nm of silicon oxide film 48 using the high density plasma is formed. Growth conditions are SiH4 99 cc/min, O2 237 cc/min, and 400kHz source power. It grows up at 4400W, 13.56MHz, substrate bias power 2500W, and the growth temperature of 450 degrees C.

Refer to drawing 15 .

[0048] Next, at a process (j), dry etching of the silicon oxide film 48 is carried out that opening of the contact aperture with the above mentioned polish recon plug should be carried out using a photoresist as a mask. In this contact aperture, a CVD method is used, polish recon is embedded, and it connects with a lower polish recon plug and an electric target. In this case, the inside of a contact aperture is embedded, and 1 ** deposits polish recon on more than sufficient thickness, and it is removed and plug-ized by CMP (chemical machinery-polish) later.

Refer to drawing 16 .

[0049] Then, although patterning formation of the are recording electrode 51, a dielectric film 52, and the counterelectrode 53 is carried out one by one and considered as the cel capacitor structure at a process (k), the formation procedure in this case is not different from the case of the conventional technique. Then, 2000nm of silicon oxide film 58 is formed with the CVD method using the high density plasma. Growth conditions are SiH4 99 cc/min, O2237 cc/min, and 400kHz source power. 4400W and 13.56MHz Substrate bias Power 2500W, growth temperature of 450 degrees C.

Refer to drawing 17 .

[0050] At a process (l), opening of the deep contact aperture 60 for making wiring connection with a substrate is carried out. What is necessary is just to perform opening of the contact aperture 60 in RIE (reactive ion etching). Then, the barrier metal layer 61 is first formed thinly so that it may extend on the silicon oxide film 58 from the inside of the contact aperture 60. Subsequently, the tungsten (W) layer 62 is formed thickly and an aperture is buried thoroughly. The laminated structure which consists of a barrier metal layer 61 and a tungsten (W) layer 62 is used as a conductive plug 63.

[0051] In addition, B (boron) and P (Lynn) which are contained in the BPSG film are incorporated in the BPSG film in B-2 O3 and the form of P2O5, respectively. It depends for the physical device at the time of the BPSG film carrying out a reflow at low temperature on membrane structure being distorted and association becoming easier to go out at low temperature by incorporating each above-mentioned impurity in the film. Low temperature-ization of reflow temperature can be attained by including the atom of more B (boron) and P (Lynn) because [this]. When an aspect ratio embeds four or more clearances using this invention, the thing to perform in the steam ambient atmosphere whose membrane formation conditions at the time of embedding are 700 degrees C, then B(boron) 3.7% of the weight, the concentration beyond P(Lynn) 4.7 % of the weight is needed, and if not weight % but mol% is used for the index which shows reflow nature, the total high impurity concentration in above-mentioned conversion becomes 24-mol%.

[0052] The above is explanation in alignment with 1 operation gestalt of this invention. In addition, it

cannot adhere to the example shown with the above-mentioned operation gestalt, but the conditions in a production process, an ingredient kind, etc. can be suitably changed into this invention. For example, the same effectiveness could be acquired even if it is the mixed-loading device of two or more logic block with which it can also use for the mixed-loading device of a flash memory and logic, and design sizes differ, although the mixed-loading device of DRAM and logic was taken up as optimal operation gestalt. Moreover, fundamental effectiveness can be acquired by adopting this invention, even if it is a DRAM simple substance and is a logic simple substance, and even if it is a flash memory simple substance and is a FRAM simple substance, the same fundamental effectiveness can be acquired.

[0053]

[Effect of the Invention] According to this invention, the insulator layer which is prepared on the active region on a substrate and which contains a conductive impurity, for example to the clearance between four or more high aspect ratios by flow and pressure requirement which is different so that it may become low voltage in high voltage and the back at the beginning If it grows up continuously, without stopping material gas, the formation of a volume phase leading to exfoliation is avoidable. Moreover, even if there is no prolonged heating reflow, a slit can be filled finely, adverse effects, such as heat stress and impurity diffusion beyond the need, can also be done to other elements of an active region or a component, and, in the case of a detailed device, the yield and dependability can be raised generally especially.

[Translation done.]